A high speed pixelated electron detector enabling <14 microsecond scanning diffraction readout and online data reconstruction

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A vast array of new experimental modalities have been enabled in the past several years through the development of reliable pixelated detectors synchronized to probe scanning electronics to acquire the rich information present in the central portion of the convergent beam electron diffraction pattern as a function of probe position. These 4-dimensional (or more) datasets can be readily exploited for phase contrast ptychographic imaging [1], nanoscale strain mapping [2], unit cell resolution quantitative scanning position averaged convergent beam electron diffraction [3], and more. While such detectors are now commercially available from several manufacturers with single electron sensitivity, they are typically limited to approximately 1 millisecond (1 kHz) readout times while conventional integrating-detector HAADF STEM image data is acquired at approximately 0.01 millisecond (100 kHz). This speed constraint places significant limits on accessible fields of view at high resolution due to sample drift and limits in-situ acquisition to a 4D frame rate of ~1 minute.

We present here the development of a CMOS Active Pixel Sensor that consists of a 576 x 576 array of 10 µm pixels of a design related to the original TEAM detector [4] and an outer HAADF detector with 16 concentric quadrants diodes (64 elements). Data from these sensors will be digitized locally and sent over 96 multi-gigabit optical links to 4 Field Programmable Gate Array (FPGA) modules for packetization and routing. All data will be transported in real time via a 400 Gbps 1 km optical link to the Cori supercomputer at the National Energy Research Scientific Computing Center (NERSC), which will perform the 4-dimensional reconstruction and HDF5 file writing before additional asynchronous processing and analysis. This is an end-to-end development which encompasses the detector, data transportation and real-time data processing. By design this is a parallel computational workflow, and NERSC's HPC provides concurrency and a rich software environment to scale up analysis and feedback codes.

The 400 Gbps bandwidth will initially limit the frame rate to 75 kHz, and higher rates will be obtained via in-hardware edge-computing on FPGA devices to carry out the first stage of data processing before the data is placed on the network. Compression factors of more than 100 are expected when analog signals from the detector are converted to electron events, often referred to as electron counting. Machine learning routines based on convolutional neural networks are under development for more reliable and efficient detection and clusterization of electron strikes on the detector. Standard STEM image reconstructions like the integrated intensity of the bright and dark field signals as a function of scan position may also be calculated at the detector in firmware and provide instantaneous feedback to the user. More resource intensive data processing and reduction algorithms and phase contrast imaging methods such as matched illumination and detector interferometry [5] and ptychography will be performed at NERSC with the goal of near-live asynchronous feedback to the user. [6]

References:

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